S- Parameter based Analysis of substrate coupling in NMOS Transistor for Analog/RF circuit

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Abstract:
Substrate noise issues are important for the smooth integration of analog and digital circuitries on the same die. The substrate coupling mechanism with simulation and measurement in a 0.13µm common source NMOS is demonstrated. The coupling mechanism is related with resistance of ground interconnects; also the importance of coupling mechanism is demonstrated and equivalent circuit of the MOSFET with S-parameters analysis is also proposed.

1. Introduction: In the modern world the manufacturers of mobile phone are putting more and more digital and analog features day by day. This development forcing to have large number of chips on single PCB to be fabricated, and to do the proper routing and interconnection in between them is very expensive and need more power to operate. Therefore the semiconductor industries are moving towards to integrate analog and digital functionality on same die, or SoC [1]. This cost effective solution has problem of crosstalk from noisy digital part to sensitive analog part through the common substrate, this is also known as the substrate noise problem or substrate coupling [1]. This noise first generated from digital part and then propagated to all the other part of the die and also has significant impact of the functionality of the system. The generation of substrate noise can be model by modeling of digital switching noise injecting in to the substrate this can also be measured [3,4].
The different generation mechanisms in a single transistor are carefully modeled [4]. The propagation of substrate noise requires the modeling of the substrate with Electromagnetic (EM) simulator, and then modeling of the impact of substrate noise on the analog circuitry.
Analog/RF design is malfunctioning because of substrate noise coupling in analog/RF circuit. At low frequencies, where capacitive and inductive effects can be neglected, substrate noise can only resistively couple into the transistor. This resistive coupling can be by resistively into the bulk of the transistor and resistively into the p+ guard ring of the transistor. But at higher frequencies capacitive and inductive coupling also has impact on the circuit performance [5]. In this paper the simulation and the measurement for inductance (for inductive coupling) and impedance (for the capacitive coupling) is given on a dedicated test structure. The simulation model, coupling mechanism and measurement are given in different section of this paper.

2. Substrate modeling to analyze the coupling Mechanism:

In conventional bulk processes, either a heavily doped substrate with a lightly doped epitaxial layer on top or a uniformly lightly doped substrate is used. The heavily doped substrate may be modeled with less effort than a lightly doped substrate. The heavily doped silicon can be approximated to a single node due to its high conductance [7]. Therefore, the noise in highly doped substrate tends to be approximately uniform. However, the lightly doped substrate requires a higher modeling effort.

2.1 Substrate model based on Maxwell's equations:

To predict the coupling between circuits that is on the same chip a reliable substrate model is required. The substrate height dimension is not negligible with respect to the area of the silicon. Consequently, the model of the substrate must be based on the three dimensions of the substrate. The basic
Maxwell's equations can be used to find equations that can describe the substrate. However, a closed form solution does not exist as soon as geometries of different doping levels are included in the

substrate or if different layers of the substrate have different doping levels [7, 8]. For this reason, the substrate is divided into a number of smaller elements where each element is assumed to have a constant doping level. Hence, each element has a constant resistivity and a constant permittivity. The equations can then be solved so that a model of an element is achieved. If the magnetic field is ignored, a simplified form of Maxwell's equations may be used on each element [9, 10, 11].

The continuity equation

$$\varepsilon \frac{\partial}{\partial t}(\nabla . E) + \frac{1}{\rho}\nabla . E = 0 \qquad (2.1)$$

or

$$\nabla . \left(\sigma \nabla \phi(x,y,z,t)\right) + \frac{\partial}{\partial t}\left(\nabla . \left(\varepsilon \nabla \phi(x,y,z,t)\right)\right) = 0 \qquad (2.2)$$

For multidimensional cube.

Note: If this continuity equation is solved and consider the substrate as region of uniform material in electrostatic then this equation reduced to Laplace equation [6].

$$\nabla^2 \phi = 0 \qquad (2.3)$$

A cube shaped element with the volume V and the side $2d$ is shown in Fig. 1. The closed surface of the cube is denoted S.

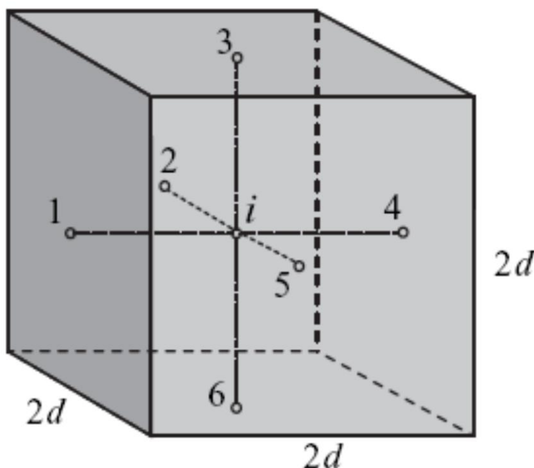

Fig. 1: A cube shaped element with the volume V and the side 2d [7]

Gauss' law gives that the divergence of the electrical field in a point equals a constant. Hence, the divergence in node i in the cube is

$$\nabla . E = k \qquad (2.4)$$

We $\nabla . E$ integrate over the volume V formed by the cube in Fig.1, and then rewrite (2.4) as

$$\int \nabla . E dV = \int_v k dV = 8d^3 k \qquad (2.5)$$

The divergence theorem gives that

$$\int_V \nabla . E dV = \int_S E dS \qquad (2.6)$$

Hence, (2.6) can be rewritten as

$$\frac{1}{8d^3}\int_S E dS = k \qquad (2.7)$$

Therefore,

$$\nabla . E = \frac{1}{8d^3}\int_S E dS \qquad (2.8)$$

The integral in (3.6) can be approximated as

$$\int_s E dS = \sum_{j=1}^{6} Eij 4d^2 \qquad (2.9)$$

And the electrical field from node j to i can be approximated as

$$Eij = \frac{Vi - Vj}{d/2} \qquad (2.10)$$

Hence,

$$\nabla . E = \frac{1}{8d^3}\sum_{j=1}^{6}\frac{Vi - Vj}{d/2}4d^2 = \sum_{j=1}^{6}\frac{Vi - Vj}{d^2} \qquad (2.11)$$

Using (2.11) in (1.1) gives

$$\sum_{j=1}^{6}\left[\frac{\left(V_i - V_j\right)}{R} + C\left(\frac{\partial V_i}{dt} - \frac{\partial V_j}{dt}\right)\right] = 0 \quad (2.12)$$

Where $R = \rho / 2d$ and $c = 2\varepsilon d$. The resulting model is shown in Fig. 2, where each impedance from a surface to the middle node *i*, is modeled as a resistor in parallel with a capacitor with the values of *R* and *C*, respectively. The expression in (2.12) corresponds to that the sum of the currents flowing into node *i* is zero.

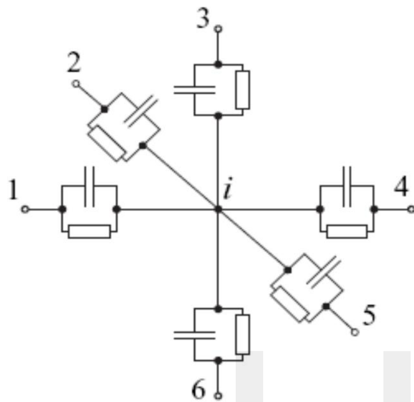

Fig. 2**:** Model of a cube shaped substrate element.

When a substrate is divided into a number of elements, a mesh of resistors and capacitors is obtained. To achieve reliable results from the model, the mesh should be fine (i.e., small elements) in regions where the gradient of the doping level is high and also where the gradient of the electrical field is high. Due to the large number of nodes required in the model, it is not suited for hand calculations and therefore a simulator is required. By using a circuit simulator (e.g., SPICE) the coupling between different areas of the substrate can be analyzed. The areas of the substrate that are of interest are often called ports in the literature

2.2 Analytical Resistance Calculation between Two Contacts

This section provides analytical formulas to extract the substrate resistance between two contacts. Those analytical formulas give how the current flows into the substrate but are restricted to very simple geometrical structures like two rectangular or circular contacts [5, 13]. The resistance between two rectangular contacts is discussed from the point of view of the substrate noise current flow. In the case of a one-dimensional current flow, the current can be considered as f owing in a floating well with two contacts at either side, or simply a resistor.

In order to calculate the resistance between the two ends of the floating well, Maxwell's equations need to be solved. Since only the resistance is of interest and a quasi-static (infinitely slow, the charges are in equilibrium) solution can be assumed, one needs to solve the first law of Maxwell, also called the Poisson equation:

$$\nabla \vec{E} = \frac{\rho_c}{\varepsilon} \quad (2.13)$$

In the case that no charges are present, the Poisson equation can be simplified to:

$$\nabla \vec{E} = 0 \quad (2.14)$$

The corresponding current density is proportional to the electrical field and inversely proportional to the resistivity of the layer (ρ_{layer}). If one assumes that the current density and the electrical field are constant across the floating n-well this becomes:

$$J = \frac{E}{\rho_{layer}} \quad (2.15)$$

The current (I) through the floating well is given by the surface (S) integral of the current density. Consider a rectangular volume with dimensions t_{layer}, w_{layer}, and d (in Fig 2.). The current I is f owing from left to right.

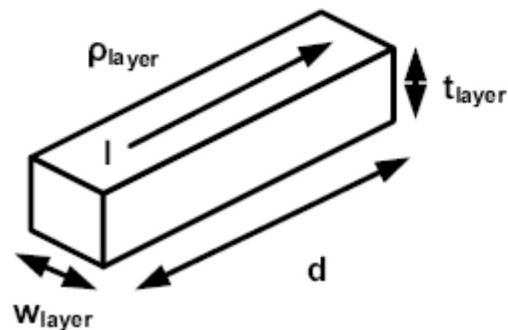

Fig. 3: Floating well with dimension *tlayer, wlayer*, and d.

In this case, the current I is equal to:

$$I = \oint\!\!\oint_S J.dS = w_{layer}.t_{layer}.j \quad (2.16)$$

Using (2.15) in (2.13) gives:

$$E = \nabla V = \rho_{layer} \frac{I}{w_{layer}.t_{layer}} \quad (2.17)$$

$$V = \int_0^d \rho_{layer} \frac{I}{w_{layer}.t_{layer}} = \rho_{layer}.\frac{I.d}{w_{resistor}.t_{layer}} \quad (2.18)$$

Then the resistance value depends on the length of the resistor (d) and its area

$$R_{resistor} = \frac{V}{I} = \rho_{layer}.\frac{d}{w_{resistor}.t_{layer}} \quad (2.19)$$

In this case, there exists a linear relationship between the resistance between two contacts and the distance between those contacts the relation is shown as result (fig 13). ρ_{layer}/t_{layer} is also called the sheet resistance Rsheet. The sheet resistance is typically used to calculate the resistance of rectangular sheets of material in terms of number of squares. In the case of two-dimensional current flow, the resistance depends on the distance over size ratio

2.3 Current Measurement:

Since the well may interact with substrate in two ways **i)** capacitively, through the source (drain)-to-substrate junction; **ii)** resistively through hot-electron injection also known as impact ionization [6, 15]. Impact ionization caused by electron hole pairs generated in the pinch-off region, when the electric field exceed a given threshold. In the NMOS transistor case, while the electrons contribute to channel current, the excess holes are collected in the region of substrate under the device and they are transported through the chip. The impact ionization current are evaluated as

$$I_{impact} = \int_{Es}^{Em} I_d A e^{-B/E(x)} dx \quad (2.20)$$

Where Es, Em, E(x), and Id are source electric field, maximum electric field, local electric field, and drain current respectively. A and B are material related constant.

If Em>>Es

$$I_{impact} = \frac{A}{B} l E_m I_d e^{-B/E_m}$$

$$= C_1 \left(V_{ds} - V_{dsat}\right) I_d e^{-\frac{C_2}{\left(V_{ds} - V_{dsat}\right)}} \quad (2.21)$$

Where *l*, V_{ds} *and* V_{dsat} are the effective channel length, drain to source voltage and saturation voltage

Previous research suggests that the impact ionization is the prominent cause of substrate noise in NMOS up to 100 MHz Impact ionization can be termed as drain to body transconductance g_{db} for small signal analysis

$$g_{db} = \frac{\partial I_{sub}}{\partial V_D} = \frac{C_2 I_{sub}}{\left(V_{ds} - V_{dsat}\right)^2} \quad (2.22)$$

The current I injected into the substrate at low frequency due to applied voltage V_{in} is given by

$$I = \sqrt{\frac{j\omega C}{R}} Tanh\left(\frac{\sqrt{j\omega RCl}}{2}\right) V_{in} \quad (2.23)$$

Assumed that one end of resistor is AC grounded and input is given at one input.

Where R, C are unit resistance and unit capacitance and l is length of resistance.

2. Substrate modeling using HFSS:

HFSS is a software package for calculating the electromagnetic behavior of a structure. The software includes post-processing commands for analyzing this behavior in detail. Using HFSS, Basic electromagnetic field quantities and, for open boundary problems, radiated near and far fields; characteristic port impedances and propagation constants; generalized S-parameters and S-parameters renormalized to specific port impedances can be computed. Generally, the properties of a physical system can be described by partial differential equations as, e.g., in the previous section. A problem with this approach is that the equation system can be hard or impossible

to solve analytically. In the finite element method (FEM) the objects are divided into a number of elements, where the equation system in each element can be numerically solved. The finite element method is used in the commercial tool FEMLAB, which can model and simulate physics in 3D. Here, a mesh of finite elements is generated and the partial differential equations of each element are then solved. In this work HFSS is used to model lightly doped substrates. Two circuits with surfaces of 50 by 50 located on a substrate. The substrate backside is assumed to be metalized. The silicon resistivity and the relative permittivity are assumed to be 20 and 11.8, respectively. A mesh, is then generated of the substrate is made finer near the circuit areas than near the bottom of the substrate. The generated mesh consists of approximately elements. To estimate the substrate coupling, a sinusoidal signal is applied on one of the circuits. The other circuit and the backside are grounded. In The currents obtained from the simulation are used to calculate the resistive and the capacitive coupling.

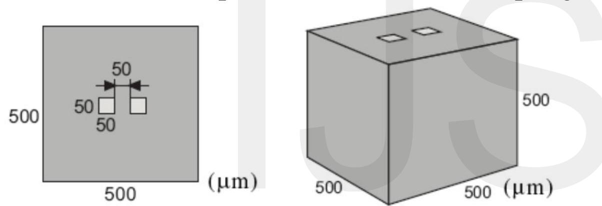

Fig. 4: A lightly doped substrate with two circuit regions of 50 by 50 μm and a metalized backside.

3.1 Pure resistive substrate modeling:

For low frequencies the substrate can be approximated as purely resistive, the substrate is mainly resistive for frequencies below the cut-off frequency.

$$f_c = \frac{1}{2\pi\rho_{sub}\varepsilon_{Si}} \quad (3.1)$$

Assuming a lightly doped substrate with a resistivity of 0.10 Ωm leads according to that the substrate is mainly resistive for frequencies up to 15 GHz. If the capacitive coupling can be neglected the model is reduced to a resistive net. Consequently, the complexity of the net is reduced which may save simulation time.

Now if the both coupling is considered as inductive and capacitive, the impedance is plotted (fig. 10)

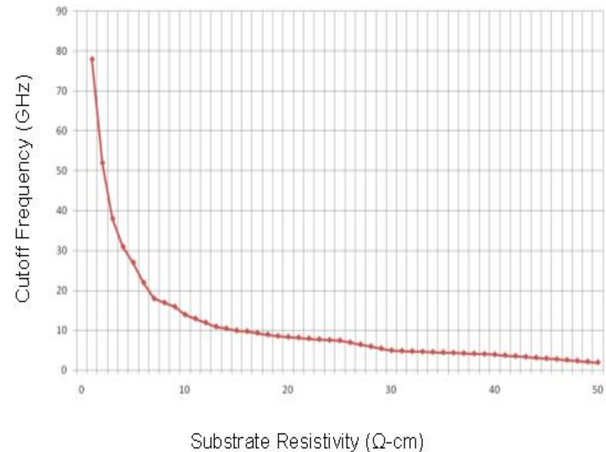

Fig. 5: variation of substrate resistivity with cutoff frequency.

4. Impact on Analog/RF circuit:

This section provides a theoretical framework to describe the substrate noise impact on analog design at the transistor level. Substrate noise has an influence on the drain current, Id, through the bulk effect and through ground bounce. The bulk effect is defined here as any perturbation on the bulk terminal of the transistor. Further, ground bounce is defined as any perturbation on the ground interconnects. For the sake of qualitative reasoning, we assume that ground bounce directly affects the source terminal of the transistor. This is true since in most of the cases the transistor is connected with its source terminal to the ground interconnect. The drain current is given by the following equation.

$$I_d = \frac{\mu CoxW}{2L}\left(V_{gs} - V_t\right)^2 \quad (4.1)$$

And the threshold voltage V_t equals:

$$V_t = V_{to} + \gamma.\left(\sqrt{|-2\phi + V_{SB}|} - \sqrt{|2\phi|}\right) \quad (4.2)$$

Where V_t, V_{t0}, γ, *and* V_{SB} *are the threshold voltage, threshold voltage at zero substrate bias, substrate bias coefficient, souse to substrate voltage.*

A Taylor expansion of (4.2) shows that V_t to first order depends linearly on V_{SB}:

$$V_t = V_{to} + \frac{1}{2}\frac{\gamma}{\sqrt{2\phi}}.V_{SB} \qquad (4.3)$$

From (4.1) and (4.2), one can notice that the drain current depends both on the voltage on the source terminal and on the bulk terminal. The drain current depends on the substrate voltage through V_{SB}. Further it is obvious if the circuit suffers from ground bounce caused by substrate noise, the drain current through V_{GS} and V_{SB} will be affected.

The drain current, I_d, is primarily defined by the nominal operation conditions of the transistor. Hence the total drain current can be defined as the sum of the nominal drain current and the variation of the drain current caused by substrate noise:

$$I_d(tot) = I_d(nom) + \Delta I_d \qquad (4.4)$$

Where $I_d(tot)$ and $I_d(nom)$ are the total and nominal currents respectively.

Where $\Delta I_d << I_d(nom)$ because substrate noise is a small signal phenomenon.

ΔI_d can be written as:

$$\Delta I_d = \frac{\partial I_d}{\partial V_{GS}}.\Delta V_{GS} + \frac{\partial I_d}{\partial V_{BS}}.\Delta V_{BS} \qquad (4.5)$$

$$\Delta I_d = g_m.\Delta V_{GS} + g_{mb}.\Delta V_{BS} \qquad (4.6)$$

Where; V_{GS}, V_{BS}, g_m are the gate to source voltage, source to substrate voltage, transconductance and g_{mb} the body transconductance of the transistor. Remember that ΔId is the unwanted variation of the drain current caused by substrate noise. Hence, the gate voltage Vg is equal to zero, and (4.6) can be rewritten as:

$$\Delta I_d = \left(g_m + g_{mb}\right).\Delta V_S + g_{mb}.\Delta V_B$$

$$\approx g_m.\Delta V_S + g_{mb}.\Delta V_B \qquad (4.7)$$

Where the V_S and V_B are the source and the substrate voltages. ΔI_d may also include the other internal noises of the transistor but here the substrate noise only is the subject of the matter. So only the substrate noise is explained.

From this qualitative reasoning, it cannot be determined whether ground bounce or the bulk effect dominates because the perturbation of the source and bulk terminal depends on the transfer function from the digital circuitry (in this case, the substrate contact) toward the different terminals of the transistor. An EM simulator is needed to calculate the amount of substrate noise that reaches the terminals of the transistor. The corresponding changes in the drain current of the transistor can be calculated by the transistor model equations.

5. Description of the Device under Test and Simulation:

Here the twin well structure is proposed In order to study the different coupling mechanisms that are present for a single transistor; a simple test structure is designed.

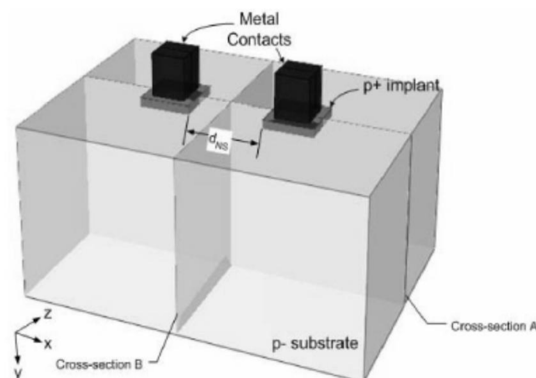

Fig. 6: transistor view in HFSS environment

The structure consists of parallel connected common-source NMOS transistors. The dimensions of the transistors are chosen large to obtain a good signal-to-noise ratio. The gate of the transistor is ESD protected for measurement purposes. Hence substrate noise can only couple capacitively through the PN junctions. Thus the ESD diodes will not influence the substrate noise coupling mechanisms into a transistor at low frequencies.

A dedicated substrate contact with a size of 114 µm by 58 µm is placed next to the transistor. A substrate contact acts as a resistive connection between the measurement equipment and the substrate. Hence, such a substrate contact can be driven by a source to replace the digital switching noise in this experiment in a controlled way.

EM simulator proved to be a very powerful tool to analyze the propagation of substrate noise. Such an EM simulator only solves the Maxwell equations and not the drift-diffusion equations, which describe the behavior of the active devices. The behavior of the active devices is included into the RF models and hence the usage of the RF models avoids the need to characterize the active

devices all over again. In the methodology proposed here, the active and the passive part of the design are modeled separately. The active devices are described by the respective RF models. The passive part (i.e., the substrate and the interconnects) are described by a finite element model.
Consequently the substrate and interconnects are described by small-signal S-parameters.

5.1 Parasitic Calculation:

The S-parameter for the MOSFET in HFSS environment is first calculated which depict the isolation between the contacts. When the transistor is not conducting (the channel is not formed) the S-parameter will show the perfect isolation i.e. no power is will transfer from one contact to other. When the transistor is conducting (the channel is formed) the S-parameter value is reflected bellow the -10dB which means the 90% power will transfer from one contact to the other. The S-parameter and Y-parameter can be directly found from the HFSS tool, and then the parasitic can be calculated from the Y-parameter as;

$$Y_{11} = \frac{sCdb(1 + sR_{sub}(C_{sb} + C_{gb}))}{1 + sR_{sub}C_b} \qquad (5.1)$$

$$Y_{12} = \frac{s^2 R_{sub} C_{db} C'_{gb} \, \Delta x}{1 + sR_{sub}C_b} \qquad (5.2)$$

$$Y_{22} = \frac{sC'_{gb} \, \Delta x(1 + sR_{sub}(C_{sb} + C_{db} + C_{gb} - C'_{gb} \, \Delta x))}{1 + sR_{sub}C_b} \qquad (5.3)$$

Where $C_{db,}$ C_{sb} and C_{gb} are the drain-to-substrate capacitance, source-to-substrate capacitance and gate-to-substrate capacitance, respectively, C'_{gd} and C'_{gb} are the gate-to-drain capacitance per unit width and gate-to-substrate capacitance per unit width, R_{sub} is the substrate resistance, and C_b is the sum of $C_{gb},$ C_{db} and $C_{sb},$ where Δx is an infinitesimal section of the gate width.

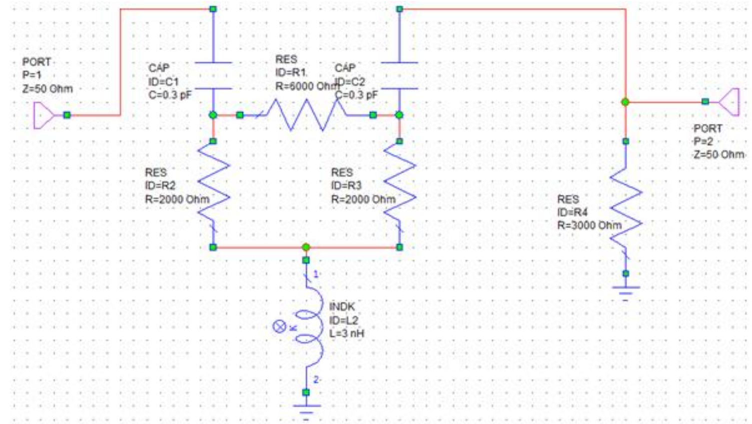

Fig.7. equivalent circuit of the transistor test structure. Equivalent lumped element circuit of the experiment setup (In AWR).

On this simulation model an S-parameter analysis is performed; when an S-parameter analysis is performed, a DC analysis is performed first. The DC operating point of the transistor is calculated based on the DC results of the S-parameter box obtained by the HFSS simulation. HFSS extrapolates the DC operating points. In this way the correct DC potential can set. The resulting simulation model is analyzed with a circuit simulator. The supplementary information about the substrate noise coupling mechanisms from both the EM and the circuit simulation can be extracted:

6. Results:

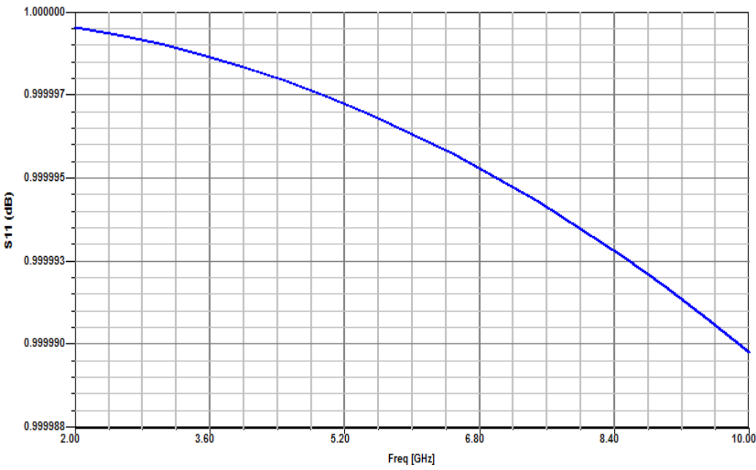

Fig. 8: S11 (dB) (return loss/isolation) simulated when the transistor is not conducting

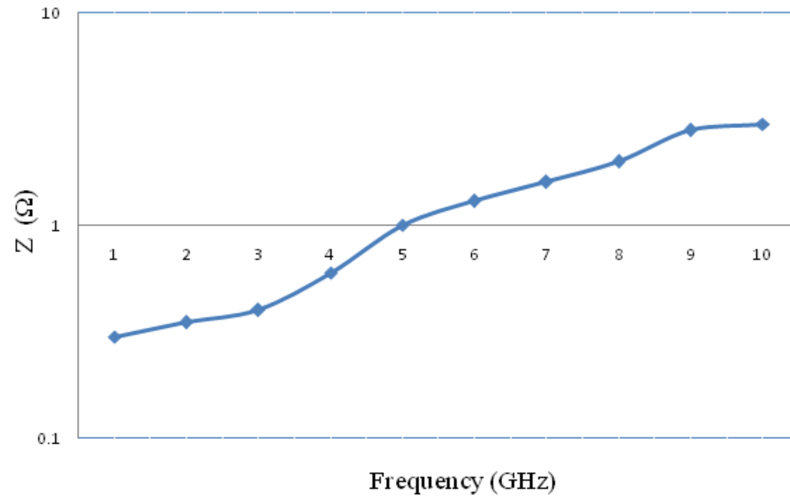

Fig. 10: Impedance variation over the frequency band (measured)

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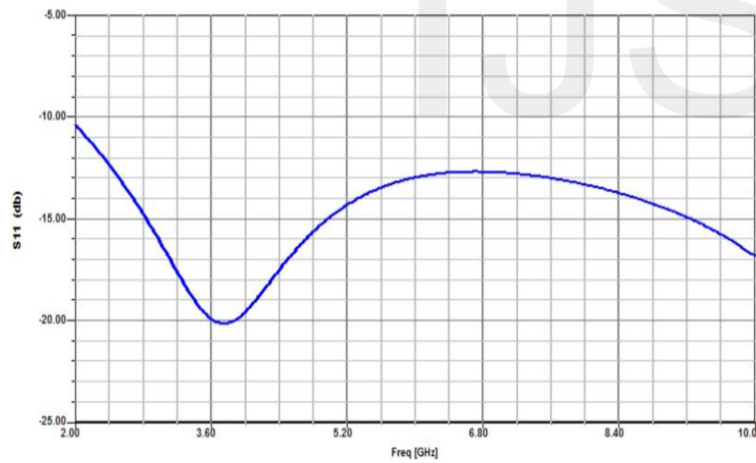

Fig. 9: S11 (dB) (return loss/isolation) simulated when the transistor is conducting

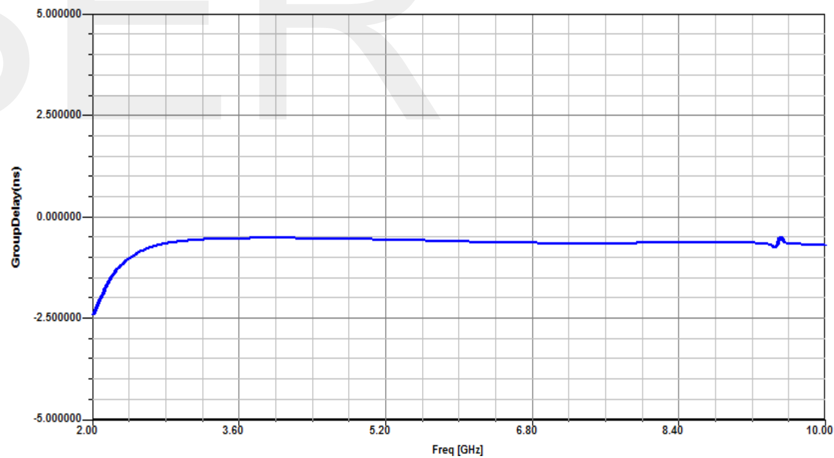

Fig. 11: Group delay (linear phase response) simulated over the frequency band between the input and output

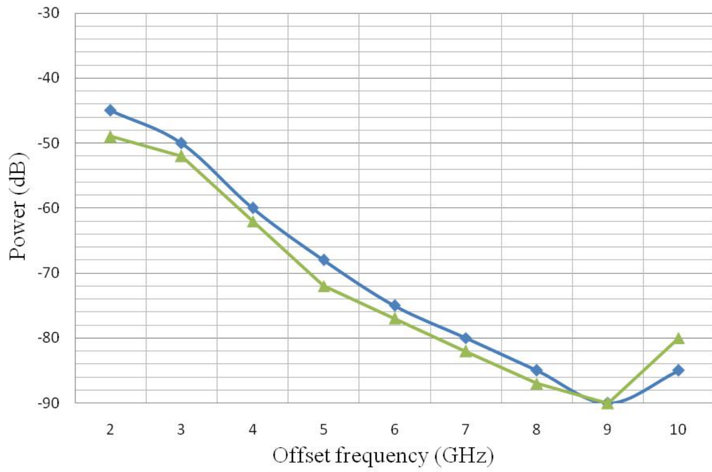

Fig. 12: Comparison of the power in (dB) at the contact for the two contacts of different sizes

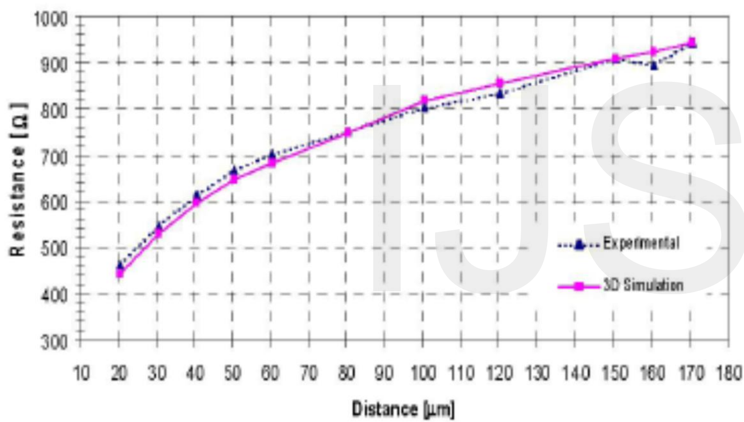

Fig. 13: Comparison of experimental and 3D simulated substrate resistance, as a function of the p+ substrate contact distance

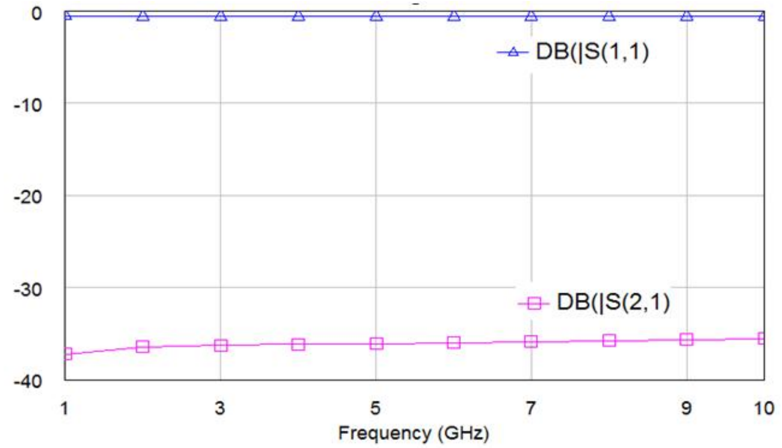

Fig. 14: Comparison of s-parameters for the design propose in [5] with the design simulated for the conducting and non conducting modes shown in Fig.8 and Fig. 9.

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Result Discussion:

The isolation in between the contacts is reflected by the S11; in fig. 8 the S11 versus frequency plot is given which is depicting that when the transistor is not conducing there is no power transmitting from the one contact to other i.e. the contact are isolated, but in the fig. 9 the S11 versus frequency; when the transistor is conducting S11 is less than -10dB over entire frequency band i.e. more than 90% of power is being transmitted. When the transistor is conducting the contacts should not be isolated and this validating by the fig. 9.

In Fig. 10, the variation of the impedance at different operating frequencies is shown; here the variation of the impedance is very less over the entire band, i.e. the impedance between input and output is perfectly matched, and in fig. 10 shows the group delay at different frequencies; the variation over the entire frequency band is about 1ns; i.e. the phase response between the input and output is linear; the variation is due to the substrate coupling but the impact is not very much for the design taken. In the fig. 12; power versus frequency for the two contacts of different sizes (50 um and 75 um) is shown at different frequency of operation. More will be contact size the noise power will be more. The resistance between the contacts is calculated by putting the contacts at different distances. The results are shown in the fig.13. As the distance between the contacts will increase the resistance between them will increase and hence the distance between the contacts must be as where the coupling is less.

8. Conclusion:

The experimental results and simulation verifications provide an understanding of the noise coupling effect of in a lightly doped silicon substrate i.e. the high substrate resistivity. Simulation results from simple test structures indicated that SOI had significantly less coupling compared to bulk. The frequency where the coupling in SOI becomes approximately the same as that in bulk is very dependent on the chip structure. Increasing the distance between the circuits was effective to decrease the substrate coupling in both bulk and SOI. The cost of increasing distance is mainly the increased area. The inductance at certain frequency for the inductive coupling is invariant and varies with the aspect ratio; and the impedance and group delay is depicting that for the design used the group delay variation is about 1ns which is because of the substrate coupling. The substrate coupling is frequency dependent; the coupling becomes prominent when frequency increases. In SOI, a substrate with a high resistivity can be used which decreases the substrate coupling up to the frequency where the capacitive coupling becomes dominating. The cutoff frequency decreases when the resistivity of the substrate increases. At last the comparison of the s-parameters for the design proposed in [5] with the design simulated in this literature.

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